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| 10/719,409 | 11/22/2003 | Frederick Curtis Furtek | NVDA/P002849 | 3361 |

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| EXAMINER | |
|---|---|
| SUN, SCOTT C | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/719,409 | FURTEK ET AL. | |
| | Examiner | Art Unit | |
| | SCOTT SUN | 2182 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,5-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-18,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 1, 5-18, 20, and 21 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1, 6, 8, 10, 12, 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian et al (pub #2002/0015401, hereinafter Subramanian) in view of Wolrich (previously cited).

4. Regarding claim 1, Subramanian discloses An adaptive computing engine (signal processing engine having configurable architecture in figure 1, details shown in the remaining figures), comprising:

a programmable interconnection network (reconfigurable interconnect 204a shown in figure 2B, described in detail in paragraphs 75, 76);

a plurality of nodes (hardware kernels K1-K6 in figure 2C), wherein each node included in the plurality of nodes has a fixed and different architecture that corresponds to a particular algorithmic function (heterogeneous structure, paragraph 73), and each node is coupled to one or more other nodes in the plurality of nodes via the

programmable interconnection network (connected by interconnect 204a, paragraph 72);

Subramanian teaches reconfigurable dataflow (paragraph 68) but does not disclose explicitly a reconfigurable IO controller. However, Wolrich discloses a reconfigurable IOC (system shown in figure 1, details shown in figure 3) coupled to a first node in the plurality of nodes via the interconnection network (various connections shown in figure 3), the reconfigurable IO controller including: at least one input coupled to the programmable interconnection network for receiving a point-to-point transfer instruction (read or write operation) from the first node (CPU); and at least one output (output from translation unit) for providing a translated point-to-point transfer instruction to an external device (devices connected to FBUS including Octal MAC 13a and Ethernet 13b; column 5, line 42-52). Teachings of Subramanian and Wolrich are from the same field of computing hardware design.

Therefore, it would have been obvious at the time of invention to combine teachings of Subramanian and Wolrich by using the IO controller of Wolrich in the adaptive computing engine system of Subramanian for the benefit of controlling and translating commands between different hardwares (column 41-46).

5. Regarding claim 6, Subramanian and Wolrich combined disclose claim 1, and Wolrich further discloses wherein a translated point-to-point transfer instruction provides translation of an address associated with the adaptive computing engine to the external device (column 5, line 42-52).

6. Regarding claim 8, Subramanian and Wolrich combined disclose claim 1, and Subramanian further discloses memory random access circuitry (paragraph 80).

7. Regarding claim 10, Subramanian and Wolrich combined disclose claim 1, and Subramanian further discloses a real time input circuitry (various communication hardware described in paragraph 44).

8. Regarding claim 12, Subramanian and Wolrich combined disclose claim 1, and Subramanian further disclose a physical link adaptor (communication links described in paragraph 41) connected to an input of the configurable IOC.

9. Regarding claim 15, Subramanian and Wolrich combined disclose claim 1, and Subramanian further discloses wherein the interconnection network enables communication among a plurality of nodes and interfaces to reconfigure the ACE for a variety of tasks (paragraph 73).

10. Regarding claim 16, Subramanian and Wolrich combined disclose claim 1, and Subramanian further discloses wherein the IOC runs at the interconnect network clock rate. Examiner notes that because the ACE is integrated with the IOC, then the nodes will run at a synchronized clock rate.

11. Regarding claim 17, Subramanian and Wolrich combined disclose claim 1, and Subramanian further discloses wherein the external devices include at least one ACE and at least one system on a chip (paragraph 85). Examiner notes that Subramanian discloses that reconfigurable circuitry can be used a variety of systems.

12. Regarding claim 18, Subramanian and Wolrich combined disclose claim 17, and Subramanian further discloses wherein the IOC includes status lines to the SOC, the

SOC being responsive to the status lines to prioritize multiple external devices (status information exchange, paragraph 78).

13. Regarding claim 19, Subramanian and Wolrich combined disclose claim 1, and Wolrich further discloses wherein the translation is of a port identified into an SOC address (column 5, lines 53-56).

14. Regarding claim 20, Subramanian and Wolrich combined disclose claim 1, and Wolrich further discloses wherein the external device includes at least one of a host computer and a central processing unit (computers connected to the Ethernet or MAC interfaces).

15. Regarding claim 21, Subramanian and Wolrich combined disclose claim 17, and Subramanian further discloses wherein the SOC includes a device chosen from a group comprising an ACE, storage system, a network access system, and a digital signal processor (wide range of uses cited in paragraph 85)

16. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolrich in view of Subramanian and further in view of Shukla (previously cited).

17. Wolrich and Subramanian combined disclose claim 1, but does not disclose explicitly translation of a port number. However, Shukla teaches translation of a port number (paragraph 52). Teachings of Wolrich, Subramanian, and Shukla are from the same field of data transfer processing.

Therefore, it would have been obvious at the time of invention to combine teachings of Wolrich and Subramanian and further with teachings of Shukla by

translating the port number to allow transferring data to different LANs such as those connected to the Octal MAC 13a or Ethernet 13b (paragraph 52).

18. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolrich in view of Subramanian and further in view of Warren (previously cited).

19. Regarding claim 7, Wolrich and Subramanian combined disclose claim 1, but do not disclose explicitly peek/poke service circuitry. However, Warren discloses peek/poke service circuitry (peek and poke; column 12, lines 37-45). Teachings of Wolrich, Subramanian, and Warren are from the same field of processors, and specifically of data transfer processing.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Wolrich and Subramanian and further with teachings of Warren by adding peek/poke circuitry in the combined system of Wolrich and Subramanian to read and write to memory contents.

20. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolrich in view of Subramanian and further in view of Kean (US Patent #5,469,003).

21. Regarding claim 9, Subramanian and Wolrich combined disclose claim 1, but do not disclose explicitly using direct memory access circuitry. However, Kean discloses direct access circuitry used with reconfigurable circuits (column 2, lines 43-47). Teachings of Wolrich, Subramanian, and Kean are from the same field of processors, and specifically configurable processors.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Wolrich with Subramanian and further with Kean by using direct memory access circuitry for the benefit of offloading data transfer operations from the main processor as support chips.

22. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolrich in view of Subramanian and further in view of Pham et al (previously cited).

23. Wolrich and Subramanian combined do not disclose explicitly a status line. However, Pham discloses a status line (grant and status signals, figure 11) coupled to an external device (other processors) for indicating an availability of services (paragraph 64). Teachings of Wolrich, Subramanian, and Pham are from the same field of processors, and specifically of data transfer processing.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art at the time of invention to combine teachings of Subramanian, Wolrich, and further with teachings of Pham by adding status lines into the combined system of Subramanian and Wolrich for the benefit of loading balancing (paragraph 64).

24. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolrich in view of Subramanian and further in view of Schunk et al (previously cited).

25. Regarding claim 13, Wolrich and Subramanian combined disclose claim 1, but do not disclose explicitly a plurality of different physical connectors coupled to the coupling circuitry. However, Schunk discloses a plurality of different physical connectors (column

8, lines 5-16). Teachings of Wolrich, Subramanian, and Schunk are from the same field of processors and specifically of data transfer processing.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Wolrich, Subramanian, and Schunk by adding multiple connectors in the combined system of Wolrich and Subramanian for the benefit of failure recovery (Schunk, column 8, lines 5-16). Examiner notes that coupling circuitry is any data carrier (data bus) between the physical link and the connectors.

26. Regarding claim 14, Wolrich, Subramanian, and Schunk combined disclose claim 13, and Schunk further discloses a reconfigurable finite-state machine (automatic protection switching hardware) for controlling the coupling circuitry to selectively connect a signal from a physical connector (column 8, lines 5-16).

## ***Conclusion***

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT SUN whose telephone number is (571)272-2675. The examiner can normally be reached on Mon-Thu, 10:00am-8pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182